REMARKS

The Examiner's Office Action of April 3, 2003 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

By the above actions, new claims 11-14 have been added. Accordingly, claims 1-14 are pending for consideration, of which claims 1 and 3 are independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 1-10 stand rejected under 35 U.S.C. §103(a) as unpatentable over the combination of Choi et al. (U.S. Patent No. 6,168,991 – hereafter Choi) and Moise et al. (U.S. Patent No. 6,534,809 – hereafter Moise). This rejection is respectfully traversed at least for the reasons provided below.

Claim 1 of the present invention relates to a method for fabricating a semiconductor device including a capacitor device composed of a lower electrode, a capacitor dielectric film, and an upper electrode. The method includes the steps wherein an upper conducting film is deposited on a lower conducting film by CVD, and the lower conducting film is deposited over a substrate by sputtering. Hence, a conducting film is formed into the lower electrode, which comprises the upper and lower conducting films that are in direct contact with each other.

According to claim 1, the film thickness of the entire conducting film, which includes the lower and upper conducting films formed respectively by sputtering and CVD, is more uniform than the film thickness of a conducting film formed solely by sputtering. As a result, during the annealing step in which the capacitor dielectric film is formed, agglomeration of the conducting film that is formed into the lower electrode is minimized. Thus, the lower electrode can be prevented from being disconnected at the bottom corners.

Turning now to Choi, the reference teaches, as shown in Figs 3-5, (a) a step of depositing a first conductive electrode layer (20), (b) a step of depositing a dielectric film (22) on the first conductive electrode layer (20), and (c) a step of depositing a second conductive electrode layer (26) on the dielectric fun (22). In addition, Choi discloses that the first and second electrode layers (20 and 26, respectively) are deposited by either sputtering or CVD.

In other words, Choi merely discloses using either sputtering or CVD, but not both, to deposit the first conductive electrode layer (20), which is a lower electrode. Hence, Choi fails to disclose the conductive film composed of the upper conducting film, which is deposited by CVD, and the lower conducting film, which is deposited by sputtering, such as in claim 1 of the present invention.

In the Office Action, the Examiner asserts that Choi discloses depositing the "first conductive layer" (20) by sputtering, and the "second conductive layer" (26) by CVD. However, Applicants respectfully assert that the Examiner has misunderstood the invention of Choi by characterizing that the first electrode layer (20) and the second electrode layer (26) in Choi respectively as corresponding to the lower conducting film and the upper conducting film in claim 1 of the present invention. The second electrode layer (26) actually corresponds to the upper electrode in claim 1 of the present invention, as there is a dielectric layer (22) sandwiched between the second electrode layer (26) and the first electrode layer (20) in Choi, but not with the upper conducting film of the lower electrode of claim 1 of the present invention.

Applicants respectfully submit that, according to Choi, the capacitor device is composed of the first conductive electrode layer (20), the dielectric film (22) and the second conductive electrode layer (26). Hence, even by combining Moise to Choi as suggested by the Examiner, it is technically impossible to deposit the second electrode layer (26) directly on the first electrode layer (20) of Choi.

Moise teaches, as shown in Fig 1, (a) a step of depositing a bottom electrode (124), (b) a step of depositing a capacitor dielectric (126) on the bottom electrode (124), and (c) a step of depositing a top electrode composed of a conductive oxide (128) and a noble metal (130) on the capacitor dielectric (126). Further, Moise discloses that the bottom electrode oxide (124), which is a lower electrode, is a laminated film composed of an Ir film and an IrO_x film. However, according to Moise, the Ir film and the IrO_x film are both deposited by sputtering (see column 9, lines 37-41). Hence, the lower electrode of Moise is different from the lower electrode in the present invention, which includes the upper conducting film deposited by CVD and the lower conducting film deposited by sputtering.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some

suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As discussed above, both Choi and Moise completely fail to disclose the step of forming the conductive film formed into the lower electrode by sputtering and CVD. More specifically, both references fail to teach, disclose, or suggest depositing the lower conducting film by sputtering and the upper conducting film by CVD. Therefore, as both references are deficient, their combination is improper in the §103(a) rejection.

With respect to claim 3 of the present invention, the claim recites an upper conducting film is deposited by CVD directly on and in contact with a lower conducting film that is deposited by sputtering; hence, a conducting film that is formed into an upper electrode includes the upper and lower conducting films.

On the other hand, as previously discussed above, Choi discloses that a second conductive electrode layer (26), which correspond to an upper electrode, is deposited by either sputtering or CVD. In other words, Choi merely discloses using either sputtering or CVD, but not both, to deposit the second electrode layer (26).

Moise discloses that a laminated film, which functions as a top electrode, is composed of an Ir film (130) and an IrO_x film (128). However Moise merely discloses that both the Ir film (130) and the IrO_x film (128) are deposited by CVD (see column 10, lines 52-55) but fails to disclose that the lower layer IrO_x film (128) is deposited by sputtering and the upper layer Ir film (130) is deposited by CVD

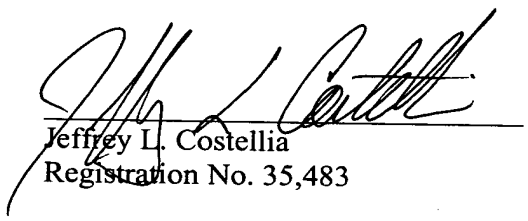
Since both Choi and Moise fail to disclose the upper electrode, which is composed of the upper conducting film deposited by CVD, and the lower conducting films deposited by sputtering, claim 3 of the present invention is clearly distinguishable over the combination Choi and Moise.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejection of claims 1-10.

New dependent claims 11-14 have been added to further complete the scope of the invention to which Applicants are entitled.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicant's representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



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